~~a~~ an first comparator responsive to a first address signal group and to first control signals, the first comparator determining when one of a plurality selected characteristics are present in the first address signal group;

A second comparator responsive to a second address signal group and to second control signals, the second comparator determining when a second of the plurality of selected characteristics is present in the second address signal group; ~~and~~

~~a second~~ an inter-comparator conductor, the ~~second~~ inter-comparator conductor applying an indicia of an identification of the second selected characteristic to the first comparator, the first comparator generating an event signal when the first and the second selected characteristics are ~~identified~~ present; and

a data qualification unit coupled to the first and second comparators, the data qualification unit receiving architecture status signals from the processor, the data qualification unit applying enabling signals to the first and second comparators.

2. (**Previously Amended**) The comparator unit as recited in claim 1 wherein the first and the second address signal groups are the same address signal group.

Please amend Claim 3 as follows.

3. **(Currently Amended)** The comparator unit as recited in claim 1 wherein the first and second selected characteristics are selected from the group consisting of an exact characteristic, a touching characteristic, a touching less than the address signal characteristic and a touching greater than the address signal characteristic.

Please cancel Claim 4.

4. **(Cancelled)** ~~The comparator unit as recited in claim 1 further comprising a data qualification unit, the data qualification unit providing an enabling signal when the data accessed by the associated address has a predetermined relationship.~~

5. **(Original)** The comparator unit as recited in claim 1 wherein either one of the first and the second comparator can generate an event signal when at least one of a touching requirement and an exact requirement is satisfied by an applied address signal group.

Please amend Claim 6 as follows.

6. **(Currently Amended)** A comparator unit for use in a test and debug system for a processing unit; the comparator unit comprising:

a first comparator and a second comparator, each comparator including:

a comparison logic unit for comparing an input address signal group with a control address signal group to determine when a selected one of a plurality of characteristics is present; and

an intercompartor conductor for providing the results in one comparator to the other comparator;

a data qualification unit coupled to the first and second comparators, the data qualification unit receiving architecture status signals from the processing unit, the data qualification unit applying enabling signals to the first and second comparator; and

an event signal generation unit, the comparison logic unit applying a signal to the event generation unit ~~and to the event signal generation unit~~ of the other comparator when the selected characteristic is identified, the event generation unit generating an event signal when the signals from the two comparators have ~~predetermined values identifying~~ identified the selected characteristic associated in ~~each comparator~~ both comparators.

Please cancel Claim 7.

7. **(Cancelled)** ~~The comparator unit as recited in claim 6 wherein each comparator includes a data qualifying unit, the data qualifying unit responsive to an input signal, the input signal determining when a pre-established signal group has certain characteristics, the data qualifying unit applying a control signal to the comparison logic unit determining whether generation of an event signal is enabled.~~

Please amend Claim 8 as follows.

8. **(Currently Amended)** The comparator unit as recited in claim 6 wherein the~~, the~~ selected characteristics are selected from a group consisting of an exact characteristic and a touching characteristic.

9. **(Original)** The comparator unit as recited in claim 8 wherein the address signal groups are the same signal group.

10. **(Previously Amended)** The comparator unit as recited in claim 6 wherein the selected characteristics are entered in the comparison logic unit by control signals.

11. **(Original)** The comparator as recited in claim 10 wherein each comparator can operate independently, each comparator capable of generating an event signal in response to at least one of a touching requirement and an exact requirement.

Please amend Claim 12 as follows.

12. **(Currently Amended)** In a host processing unit, the method of determining when a first and a second input address signal group each meets at least one selected characteristic, the method comprising:

qualifying the first input address signal group;

determining in a first comparator when the first input signal group has a first selected characteristic relative to a first reference address;

qualifying the second input address signal group;

determining in a second comparator when the second input address signal group has a second selected characteristic relative to a second reference address;

coupling the results of the first comparator and the second comparator; and

generating an output signal when the first and the second predetermined conditions are met, the output signal controlling the operation of ~~the~~ a host processor.

Please amend Claim 13 as follows.

13. **(Currently Amended)** The method as recited in claim 12 further comprising identifying the position in the program execution with a program counter signal, the program counter signal being one of the address signal groups.

Please cancel Claim 14.

14. **(Currently Cancelled)** ~~The method as recited in claim 12 further comprising applying a signal from a data qualification unit indicating that the data signal group accessed at the input address signal group has a predetermined relationship.~~

Please cancel Claim 15.

15. **(Currently Cancelled)** ~~The method as recited in claim 14 wherein the predetermined relationship is determined by the relationship to a reference data value.~~

16. **(Previously Amended)** The method as recited in claim 12 further comprising applying a signal to the comparators indicative of an associated signal group characteristic, the signal controlling generation of the output signal.

Please amend Claim 17 as follows.

17. **(Currently Amended)** In a target processor, apparatus for generating a trigger signal, the apparatus comprising:

a plurality of event signal generating units, wherein at least one of the event signal generating units is a comparator unit, the comparator unit including:

a first comparator and a second comparator, each comparator having:

a comparison logic unit for comparing an input address signal group with a control signal group to determine when one of a plurality of selected characteristics is present;

an inter-comparator conductor for communicating the results of one comparator to the other comparator; and

an event signal generating unit, the comparison logic unit applying a signal to the event generating unit and to the event signal generating unit of the second comparator when the selected characteristic is identified, the event generating unit generating an event signal when the signals from the two comparator logics have predetermined logic values;

a data qualification unit coupled to the first and second comparators, the data qualification unit receiving architecture status signals from the target processor, the data qualification unit applying enabling signals to the first and second comparators; and

a trigger generation unit coupled to the plurality of event signal generation units, the trigger generation unit responsive to at least one preselected event signal for generating a ~~an associated~~ trigger control signal, the trigger generation unit generating a trigger control signal for initiating a test procedure.

18. **(Previously Amended)** The target processor as recited in claim 17 wherein the comparator unit receives a program counter address input signal identifying the position in the program execution.

Please amend Claim 19 as follows.

19. **(Currently Amended)** The target processor as recited in claim 17 wherein one comparator receives a program counter address counter address input signal and

the second comparator receives an address signal group referenced by the program counter address.

20. **(Currently Amended)** The target processor as recited in claim 17 wherein the preselected condition is selected from the group consisting of a touching requirement, an exact requirement, a touching requirement, a touching less than the address signal requirement and a touching greater than the address signal requirement.